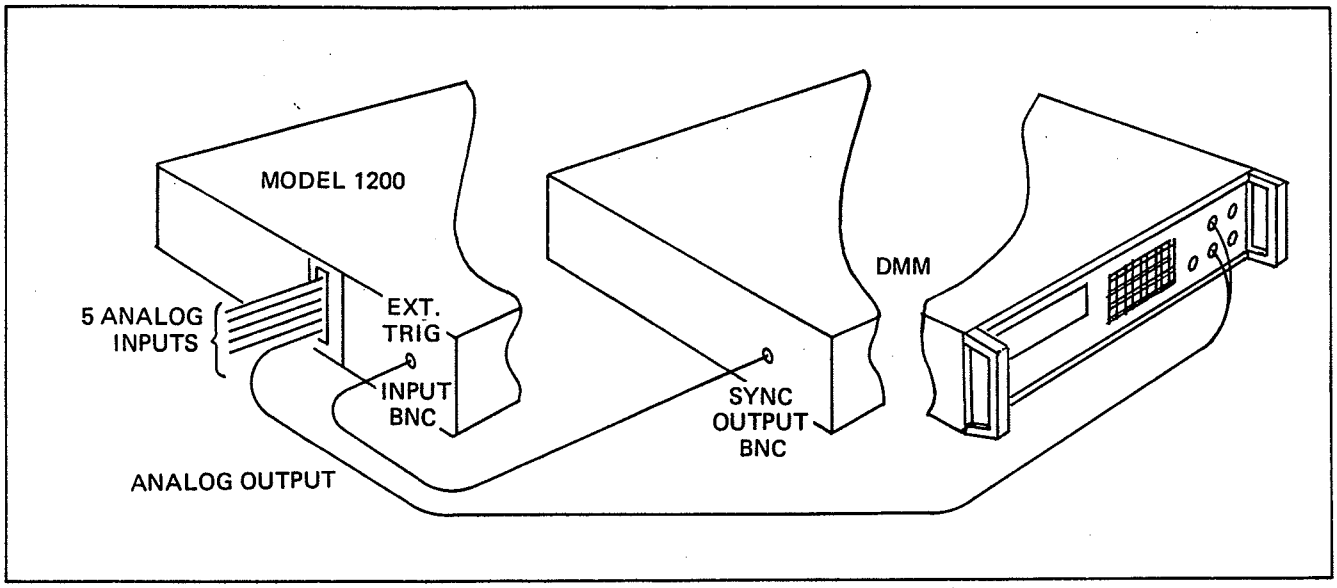


Figure 3A.2 - Signal Connections For Bench Application # 1

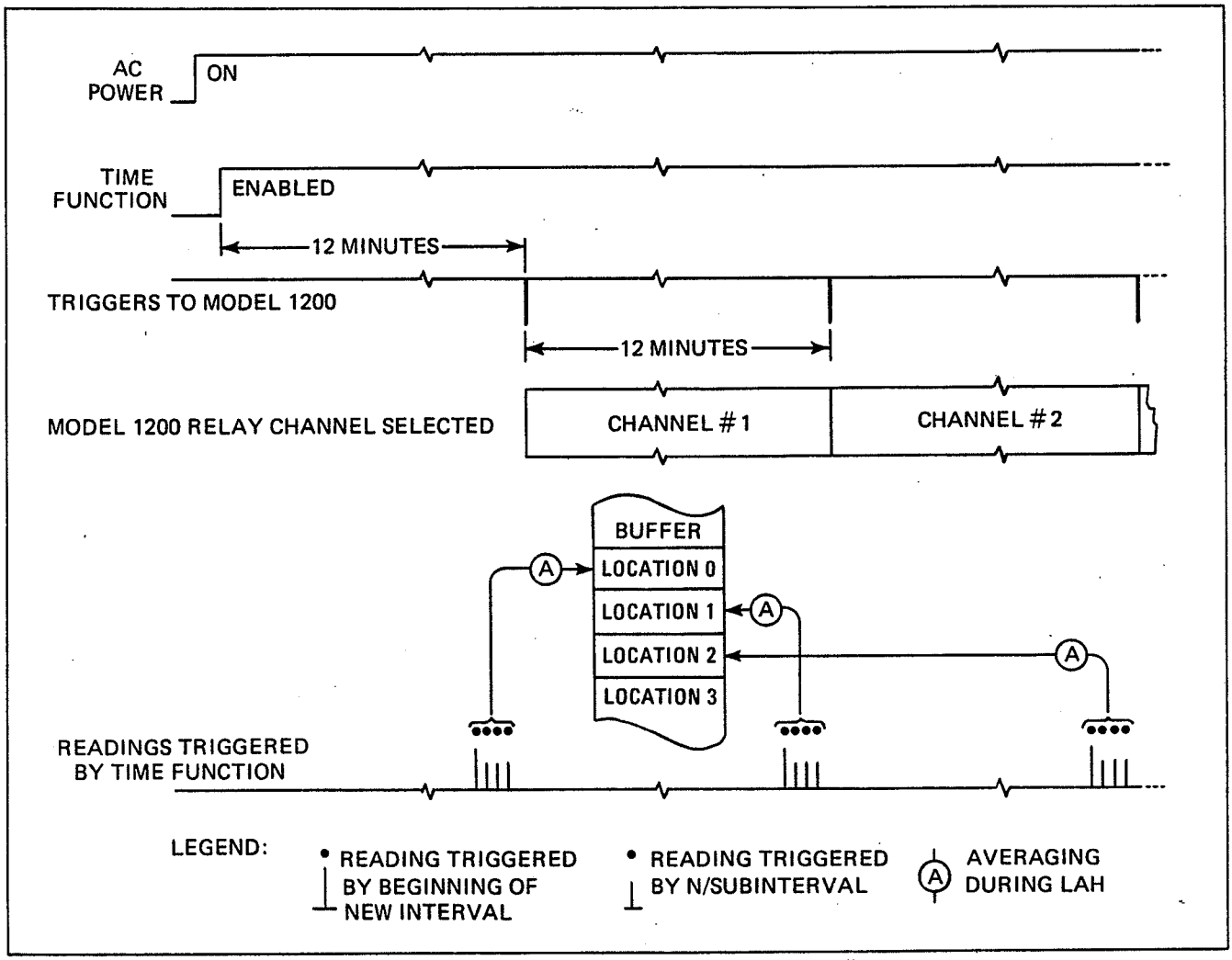


Figure 3A.3 - Read Timing For Bench Application # 1

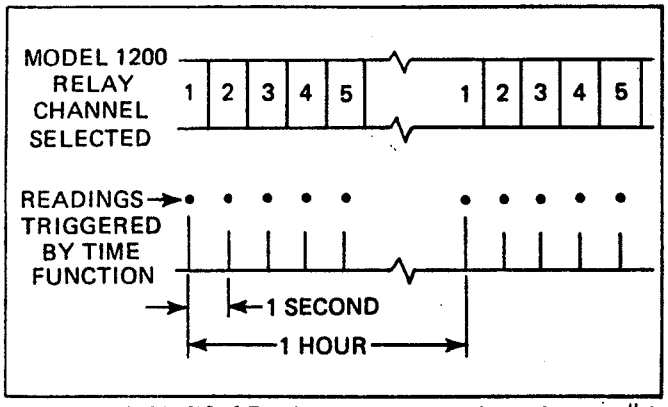


Figure 3A.4 - Modified Read Timing For Bench Application #1

3A.3 System Applications.

3A.3.1 Each System Application example contains a program listing as printed by a calculator along with an explanation for each line of the program. If the DMM is to be used with a Hewlett-Packard Model 9825 calculator the programming presented in this section may be used directly and/or further modified to suit the users needs. Because the DMM may be used with any controller which operates on the standard interface bus the user may wish to prepare equivalent software for another controller device. In such a case the user should review the remote operating instructions contained in Section 3 of this manual to select and assemble appropriate operating statements for his controller which cause the transmission of the required interface messages and device dependent messages.

3A.3.2 For example, in the first program sample in this section, line zero of the program is `rem 7` and the accompanying explanation indicates that this statement on the Hewlett Packard 9825 calculator sends the remote message to all devices on the bus. This statement causes the calculator to lower the REN line thus arming the DMM for remote operation.

3A.3.3 Referring again to the first example note that line 1 of the program printout contains the statement `flt 6` and that the accompanying explanation indicates that this sets the floating decimal format. This may or may not be a feature or function of the controller in use and since it is not an interface or device dependent message use of an equivalent is at the discretion of the user. Line 2 of the program shows the statement `wrt 702, "zF1r5"`. The explanation indicates that this transmits the device listen address 02. The user should select the statement for his controller which causes it to transmit the listen address assigned to the DMM. Instructions for the address assignment of the DMM are presented in paragraph 3.5.5. Table 3.8 shows the address switch setting, the talk and listen address characters and data line binary code for each available decimal address of the instrument.

Table 3A.1 - Key Sequence For Bench Application # 1

Step	Key Sequence	Comments
1.	SHIFT	Press the SHIFT key as required. Note SHIFT annunciator for correct execution.
2.	RESET	Clear all ESC functions.
3.	SHIFT 0 STORE TIME 1	Set start time to 0.
4.	SHIFT 9 9 STORE TIME 2	Set stop time to infinity.
5.	SHIFT • 1 2 STORE 3 TIME	Set interval to 12 minutes (= 1 hour/5).
6.	SHIFT • 0 0 0 1 STORE TIME 4	Set subinterval to 1 second.
7.	SHIFT 4 STORE TIME 5	Set N to 4 readings.
8.	SHIFT 4 STORE LAH	Set LAH Average Cycle constant to 4.
9.	SINGLE	Place instrument in Hold mode.
10.	BUFF	Clear Data Buffer by depressing Buff key until word "CLRBUF" appears on display
11.	LAH	Enable LAH and select Average by depressing LAH key until "A" appears, then release key.
12.	TIME	Enable Time function.

3A.3.4 Line 2 of the example also contains the program string which is composed of the device dependent messages. The device dependent message is the primary subject to which this section of the manual addresses itself. The examples contained in this section are presented primarily to show the various combinations of device dependent messages used to accomplish the various remotely controlled measurement operations. Note that the program printout indicates the string of device dependent messages presented in the table directly above the program tape. This format is maintained throughout the section and thus the user may use this section conveniently by referring to the device dependent message string shown for each system operation example.

3A.3.5 Line 3 of the program shown in the example instructs the DMM to become a talker and transmit the measurement data. Line 3 also instructs the calculator to store the measurement data transmitted by the DMM in a storage register known as "Variable A" and subsequentially to print the value in Variable A on the program tape. The final line on the program printout is the measurement value `7.985702e 00` the answer 7.9857 volts.

3A.3.6 The accompanying pages present eight remote systems applications, listed sequentially one through eight. Tables and figures are included throughout the examples to assist in following the explanations.

System Application #1

Purpose: Remotely program the DC volts function to measure 7.9857 volts.

Program String: ZF1R5

Device Dependent Messages

Device Code	Parameter
Z	Initialize, Internal Trigger
F1	DC Volts
R5	Range 5 (10 volts)

```
0: rem 7
1: flt 6
2: wrt 702,"zF1r
 5"
3: red 702,A
4: prt A
*9597
7.985702e 00
```

Sends Remote Enable message to all devices on the bus.

Sets floating decimal (scientific notation) format. Six places to the right of the decimal point, i.e., X.XXXXXXeXX.

Address device 02 (DMM) as listener and writes device dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).

Address device 02 (DMM) as a talker. Reads value into variable A from device 02 (DMM).

Prints the value stored in variable A.

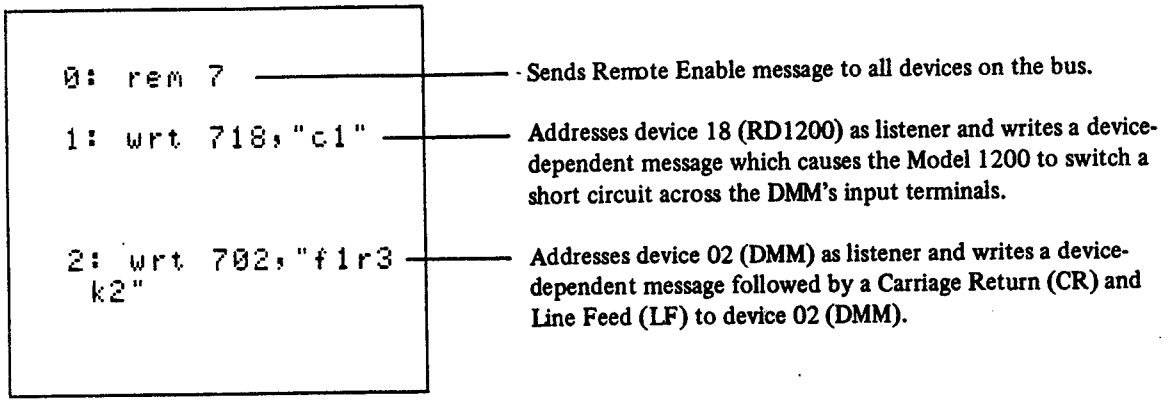
Answer: 7.9857 volts.

System Application #2

Purpose: Remotely program the DMM to zero itself against an externally-supplied short circuit, and to perform limited self-tests.

Program String: F1R3K2

Device Code	Comments
F1	DC volts
R3	Range 3 (0.1 volts)
K2	Zero command



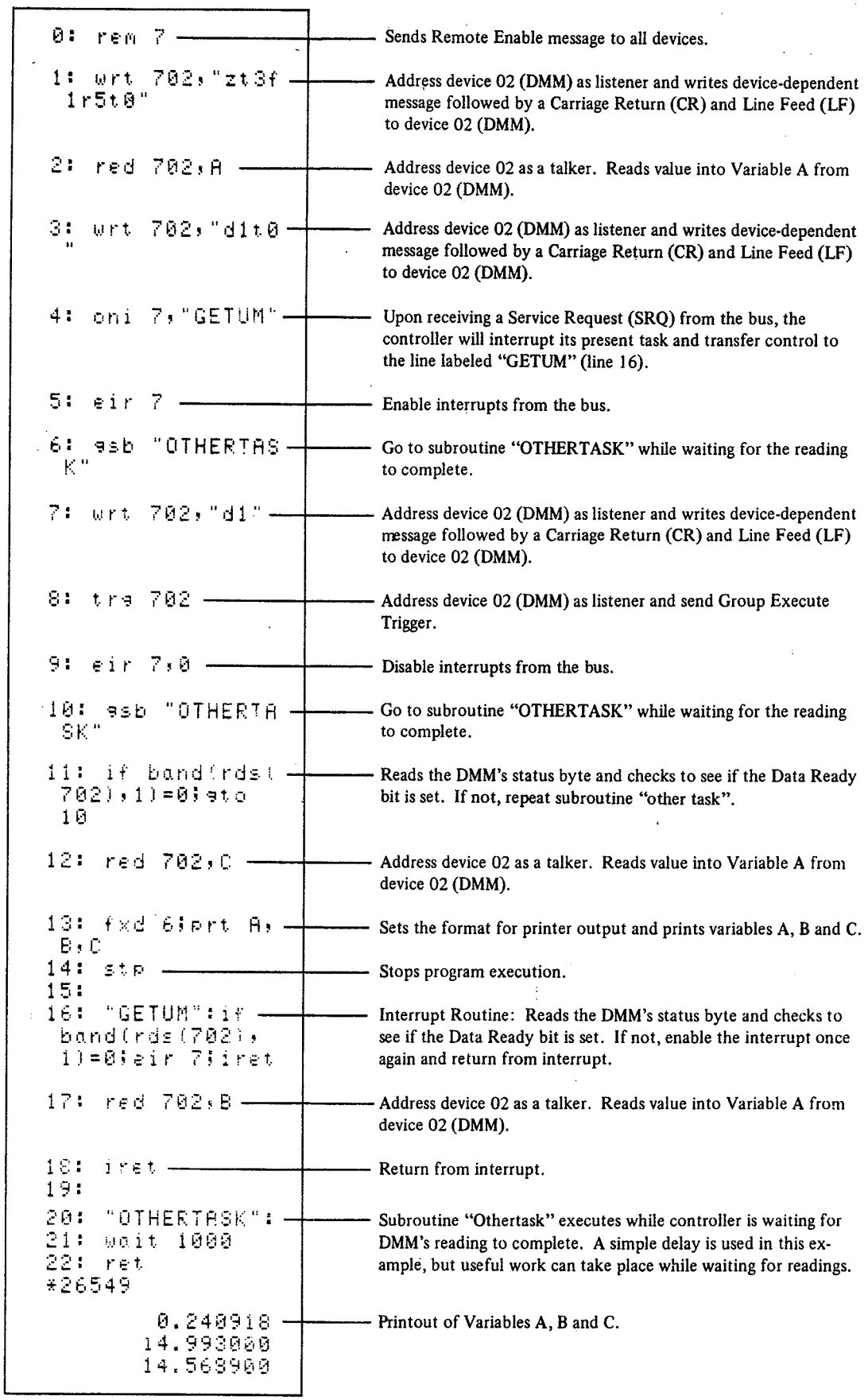
System Application #3

Purpose: Remotely program the DMM to the "Hold" mode and trigger 3 readings, each time using a different technique to trigger and/or recover the reading.

Program String: ZT3F1R5T0
D1T0
D1

Program Code	Explanation
Z	Initialize
T3	"Hold" mode
F1	DC
R5	Range 5 = 10V range
T0	Trigger 1 reading
D1	SRQ when data is ready

(No. 3 continued)



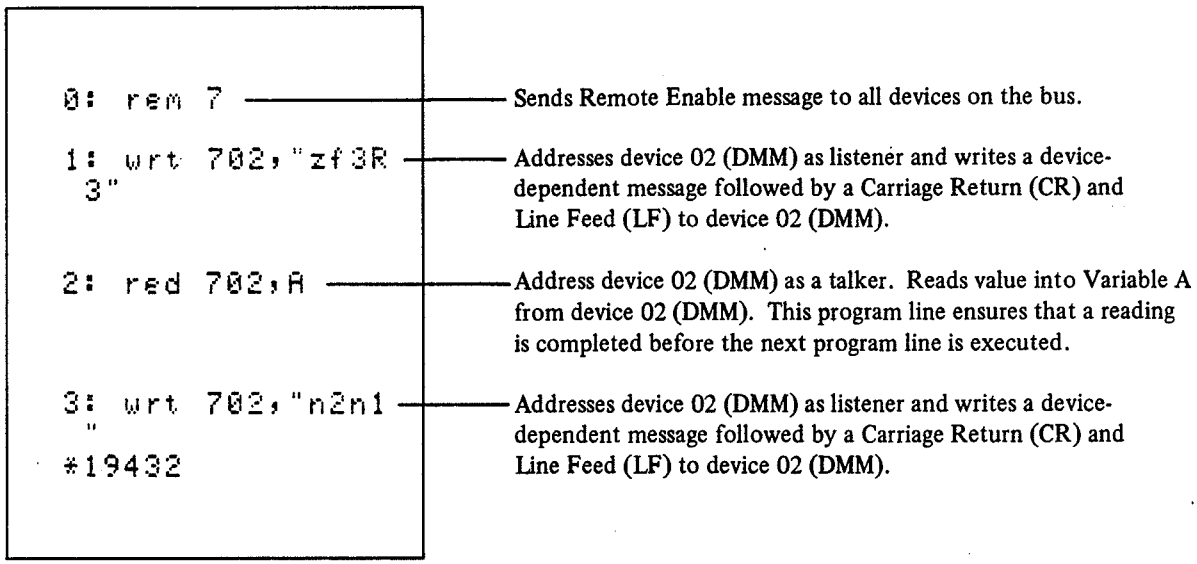
System Application #4

Purpose: Remotely program the Ohms function and compensate for (2-wire) lead resistance by storing a reference reading as the Null constant and enabling the Null function.

Program String: ZF3R3
N2N1

Device-Dependent Messages:

Device Code	Parameter
Z	Initialize, Internal trigger
F3	Ohms function
R3	0.1K Ohm range
N2	Store as Null constant
N1	Enable Null function

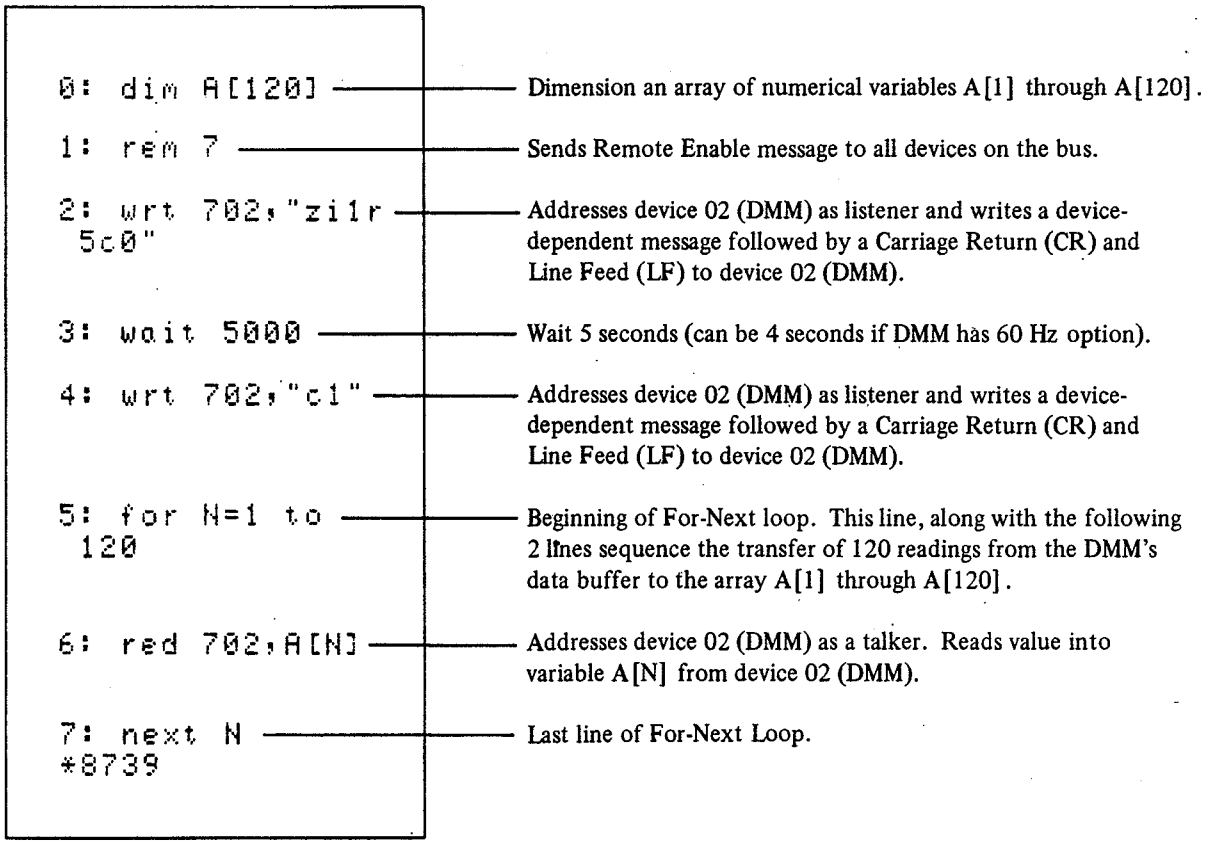


System Application #5

Purpose: Remotely program the DMM to trigger itself at high speed and store the resulting readings to the Data Buffer. The first 120 readings are then retrieved from the Data Buffer over the bus.

Program String: ZI1R5C0
C1

Device Code	Comments
Z	Initialize, Internal Trigger
I1	High-Speed Mode (4-1/2 Digits)
R5	Disable Autorange
C0	Clear the Data Buffer
C1	Output Data Buffer to GPIB

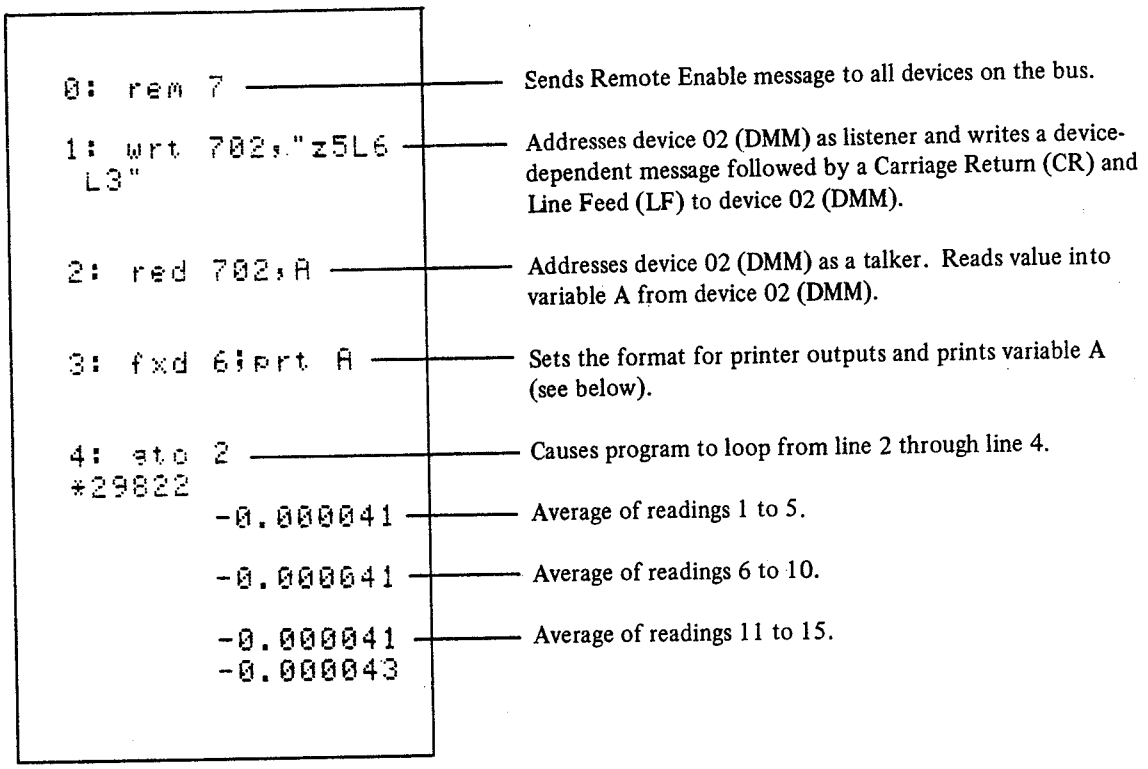


System Application # 6

Purpose: Remotely program the LAH function to average readings in groups of 5, and then output the average to the display and to the bus.

Program String: Z 5L6L3

Device Code	Comments
Z	Initialize, Internal Trigger
L6	Store Entered Constant (5.0) as the LAH Average cycle count, C .
L3	Enable LAH and select the Average as the Output.



System Application #7

Purpose: Remotely program the DMM to capture the minimum and maximum percentage deviation over a series of 10 or more readings*.

Program String: Z R5 3.75P2P1 10LGL3
L7

Device Code	Comments
Z	Initialize, Internal Trigger
R5	Range 5 (10V or 10KΩ range)
P2	Store entered constant (3.75) as the percent constant
P1	Enable Percent function
L6	Store entered constant (10.0) as the LAH cycle count C
L3	Enable LAH and select the Average as the output
L7	Transmit LAH constants: Low, Average, High, N, C

*A slow controller may have difficulty retrieving the LAH constants before an 11th reading has been completed. In this case the LAH constants will be affected by 11 readings rather than 10.

If desired, the controller can use the D1 command to cause a single SRQ to be issued after the tenth reading, thus allowing the controller's response to be interrupt-driven rather than polling the DMM as shown below.

```
0: rem 7
1: wrt 702,"zr5
 3.75p2p1 10L6L3
 "
2: red 702,A
3: wrt 702,"L7"
4: red 702,L,A,H
5: fxd 6;prt L,H
*13982
        -10.124700
         -6.364260
```

Sends Remote Enable message to all devices on the bus.

Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).

Addresses device 02 (DMM) as a talker. Reads value into Variable A from device 02 (DMM). This program line ensures that 10 readings have been completed before the next program line is executed.

Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).

Addresses device 02 (DMM) as a talker. Reads value into variables L, A and H from device 02 (DMM). Note that the L7 command made 5 numbers available for output but only the first and third are of interest in this application, therefore the 4th and 5th are not read.

Sets the format for printer output and prints variables L and H (see below).

Lowest Percentage deviation from 3.75.

Highest Percentage deviation from 3.75.

System Application #8

Purpose: Remotely program the Software Ratio and Null functions along with the Interrupt commands to do the following:

a) Configure the DMM as an AC ratiometer with a 1-10 VAC signal applied to the rear input and a 30 VAC reference connected to the front input terminals.

b) Use null along with the Interrupt commands so that the controller receives an SRQ if the ratio reading is less than 0.36.

Program String: ZF2R5V1G2Q0 .36N2N1D2

Device Code	Comments
Z	Initialize, Internal Trigger
F2	AC Volts
R5	Range 5 (10V range)
V1	Rear Input
G2	External Reference, AC function
Q0	External Reference Autorange
N2	Store entered constant (0.36) as Null constant
N1	Enable Null function
D2	Send SRQ if reading –Null is negative

```
0: rem 7

1: wrt 702,"zf2r
.5v1g2q0 .36n2n1
 d2"

2: if band(rds(7
 02),1)=0;jmp 0
*18721
```

Sends Remote Enable message to all devices on the bus.

Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and a Line Feed (LF).

Checks bit DIO1 of the serial poll status byte from device 02 (DMM). If bit DIO1 is zero (Data not ready), the line is executed again.

Execution continues on next line (not shown) if bit DIO1 of the DMM's status byte is set. This will occur only if a ratio of less than 0.36 is measured by the DMM.

SECTION 4 THEORY OF OPERATION

4.1 GENERAL.

4.1.1 This section presents the circuit description for the DMM as the signal propagates from the input terminals to the front panel display or the rear panel General Purpose Interface connector. The text will refer to simplified diagrams, schematics and other aids which may be required to enhance the general description.

4.1.2 The physical configuration drawing illustrated in Figure 4.1 is an exploded chassis view which displays the DMM main sections comprising the main PCB. The numbers identified with each section are the discussion sequence followed in the text. The DMM block diagram is presented on Figure 4.1A.

4.2 POWER SUPPLIES.

4.2.1 The DMM is designed to operate from a wide range of AC line voltages and frequencies with 120 VAC and 60 Hz considered standard. The transformer design includes a selectable multi-tapped primary winding to accommodate line voltages of 100, 120, 220, and 240 VAC ± 10%, 47 through 440 Hz. A multi-tapped secondary with three separate windings develop the low voltage DC supplies required to power the DMM circuits.

4.2.2 The primary windings are wrapped with a shield, transformer terminal 6 and the shield is connected to the DMM chassis. The chassis is connected to power line ground through the power receptacle, J209. The analog windings have two additional shields for maximum isolation and common mode rejection. The guard shield, transformer terminal 18 extends through the analog section of the PCB with two aluminum shields guarding the analog circuits. The inner shield, transformer terminal 17 is connected to analog common.

4.2.3 From the three secondary windings, low voltage DC supplies are generated to power the main sections of the DMM. The voltage levels designators and grounds appearing

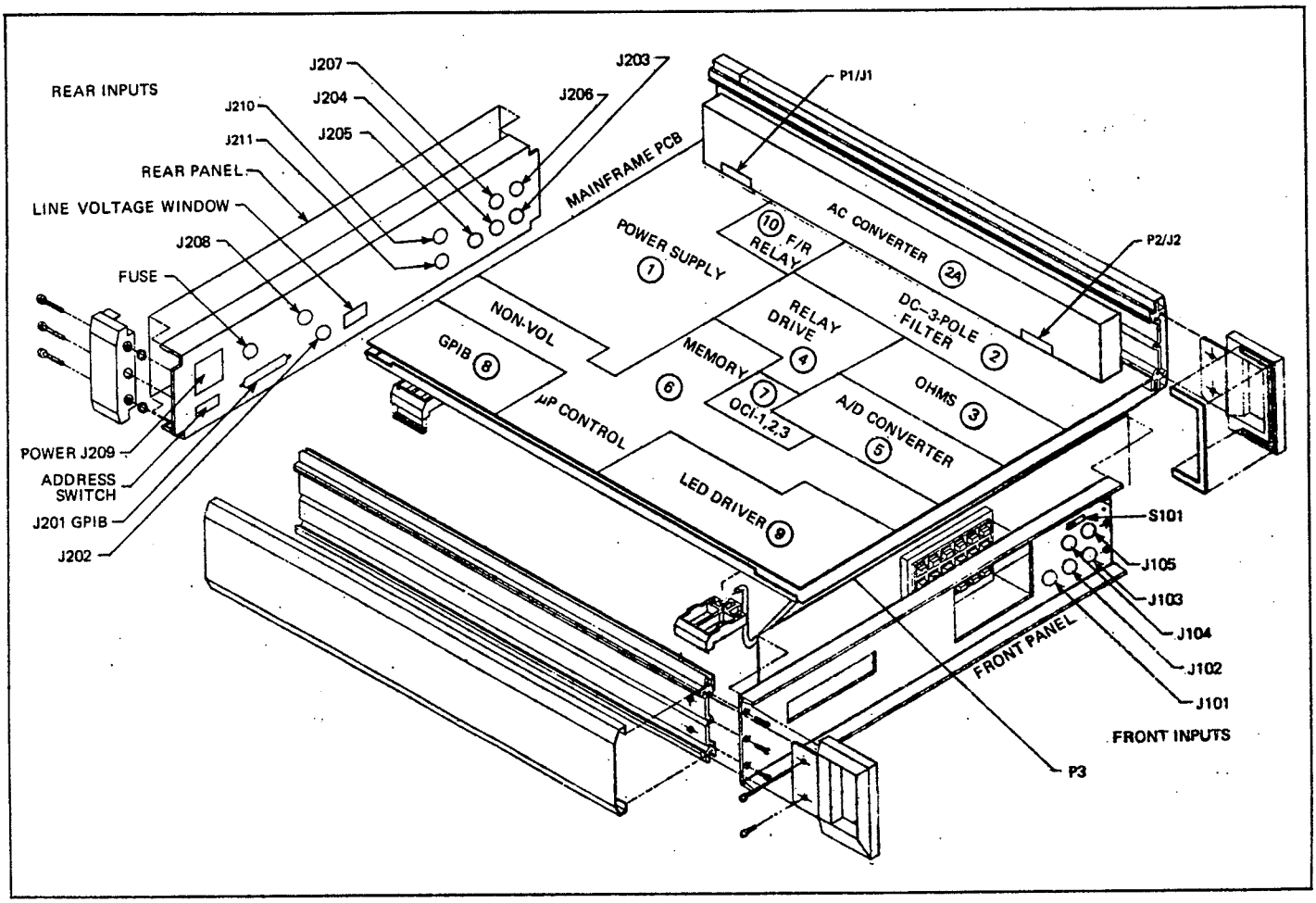


Figure 4.1 - DMM Sectional Drawing

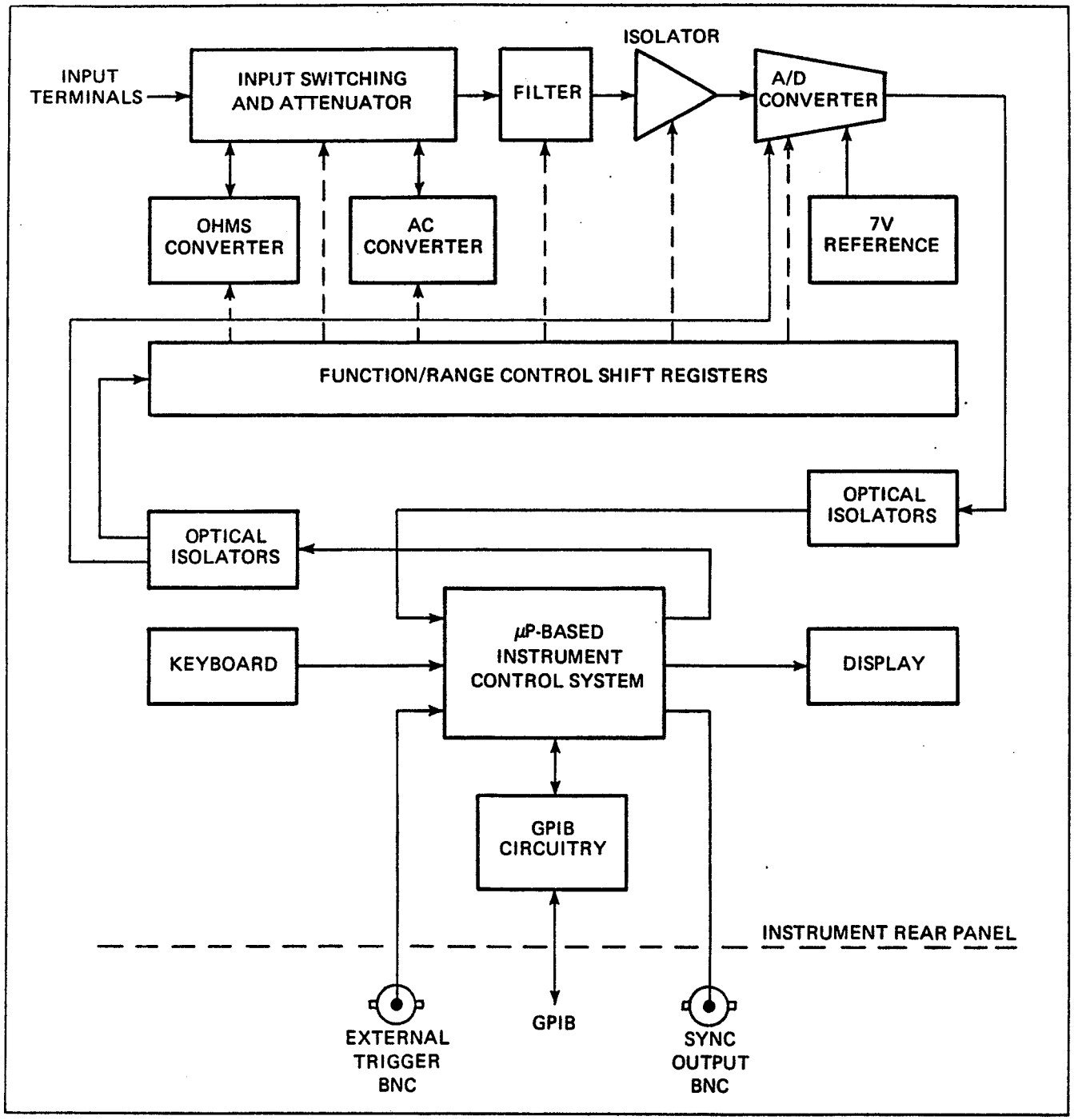


Figure 4.1A - DMM Block Diagram

on the power supply schematic, page 6-5, are used on all schematics; this is a sound troubleshooting aid.

4.3 ANALOG SUBSECTION.

4.3.1 Analog Hardware.

4.3.1.1 The Analog section of the DMM is positioned in the Guard area of the PCB assembly. This includes Section 2, 3, 4 and 5 of the board as shown in Figure 4.1, an exploded view of the DMM.

4.3.1.2 The Analog section, as shown in block diagram Figure 4.2, consists of the following basic subsections: Input Attenuator, Selectable 3-pole Active Filter, Variable gain Isolator, Variable gain AC Scaling Amplifier, True RMS or average AC converter, Ohms Amplifier and a Variable Ohms Current Source. A description for each function follows in this section.

4.3.2 Function and Range Switching.

4.3.2.1 The DMM's Function and Range are controlled by keyboard inputs, or GPIB commands. Upon receiving these signals, the microprocessor sends a new bit pattern to the function/range control shift-registers in order to energize the proper relays, and supply proper logic levels to other hardware.

4.3.2.2 The relays controlling the Function selection are K1, K8, K11 and K12. The relay closures for each function are tabulated in the following chart.

Table 4.1 - Function Relay Chart

FUNCTION	K1	K8	K11	K12
DC				
AC				▒
OHMS	▒	▒	▒	▒

▒ ENERGIZED

In the DC Function, all Function relays are de-energized and DC measurement signals are routed through the DC Input attenuator to the Isolator. In the AC Function, K12 is energized routing the input signal to the AC converter. The output signal from the AC converter is applied to the DC Input attenuator. Attenuator relay K9 is energized in AC and OHMS ranges and does not attenuate the AC converter output as the signal inputs the Isolator.

4.3.2.3 In the OHMS Function, relays K1, K8 and K11 are energized, switching the Ohms Current Source and Ohms Amplifier into the configuration shown in Figure 4.4. The Function relay chart, Table 4.1 indicates the energized relays for the Ohms Function. The ranges for DC and ohms are selected by relays K2, K3, K4, K5, K6, K7 and K9. The Range Relay chart for DC and ohms is shown in table 4.2, the next chart.

Table 4.2 - Range Relay Chart

FUNCTION	RANGE	K2	K3	K4	K5	K6	K7	K9
DC	.1V							▒
	1V							▒
	10V							▒
	100V							
	1KV							
OHMS	.1KΩ					▒	▒	▒
	1KΩ					▒		▒
	10KΩ	▒		▒				▒
	100KΩ		▒	▒				▒
	1000KΩ			▒				▒
	10,000KΩ				▒			▒

▒ ENERGIZED

This group of relays direct and scale the signal from the INPUT terminals to the Isolator input. The Isolator output signal voltage is scaled by Q15, 16, 17 and K9 as listed in Table 4.3, the Isolator Range chart.

4.3.3 DC Volt Function.

4.3.3.1 The DMM is basically a DC measuring instrument. The DC signal conditioner, which is common to AC and OHMS, performs three functions: scaling the input signal to

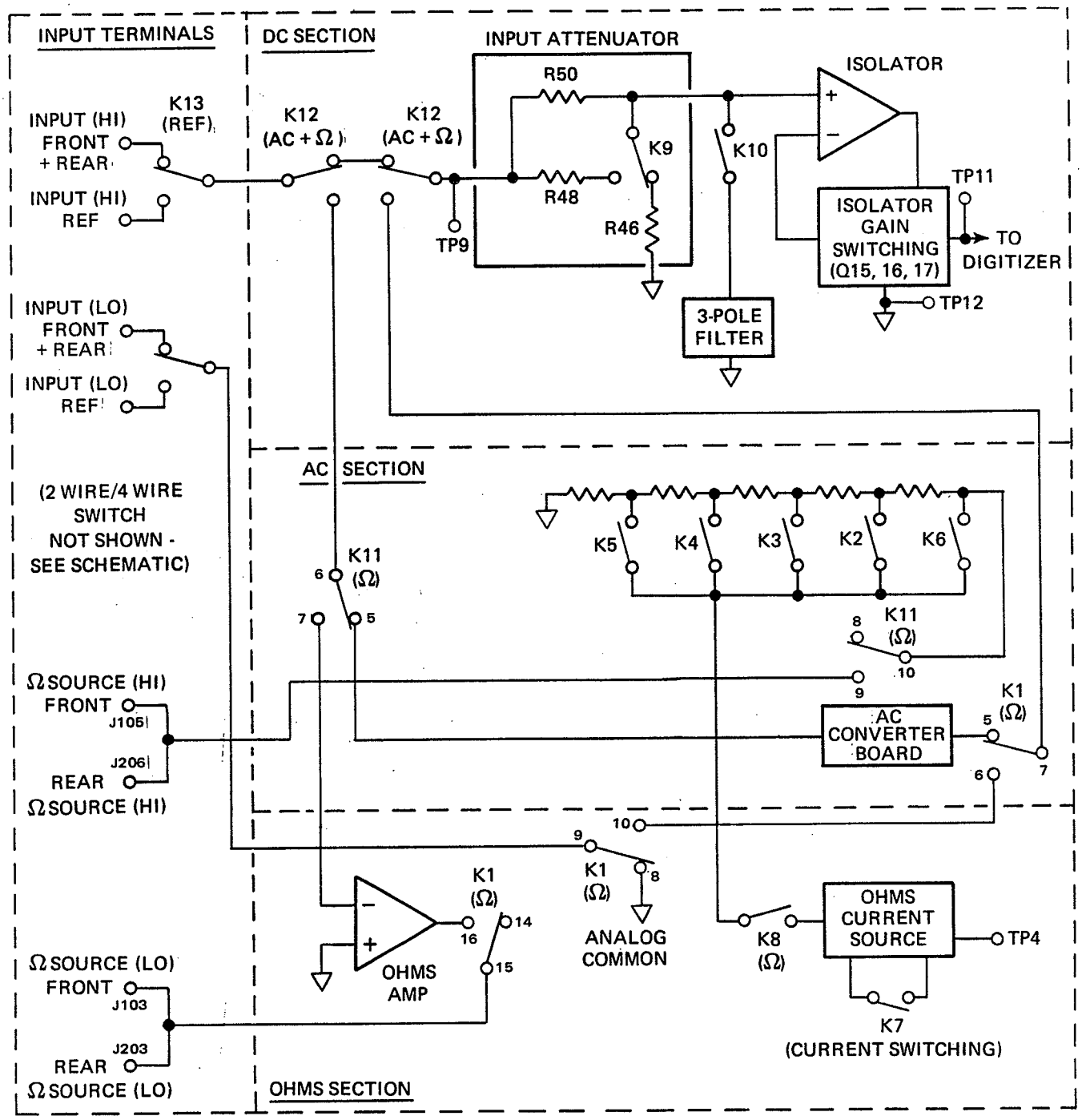


Figure 4.2 - Analog Signal Conditioning Block Diagram

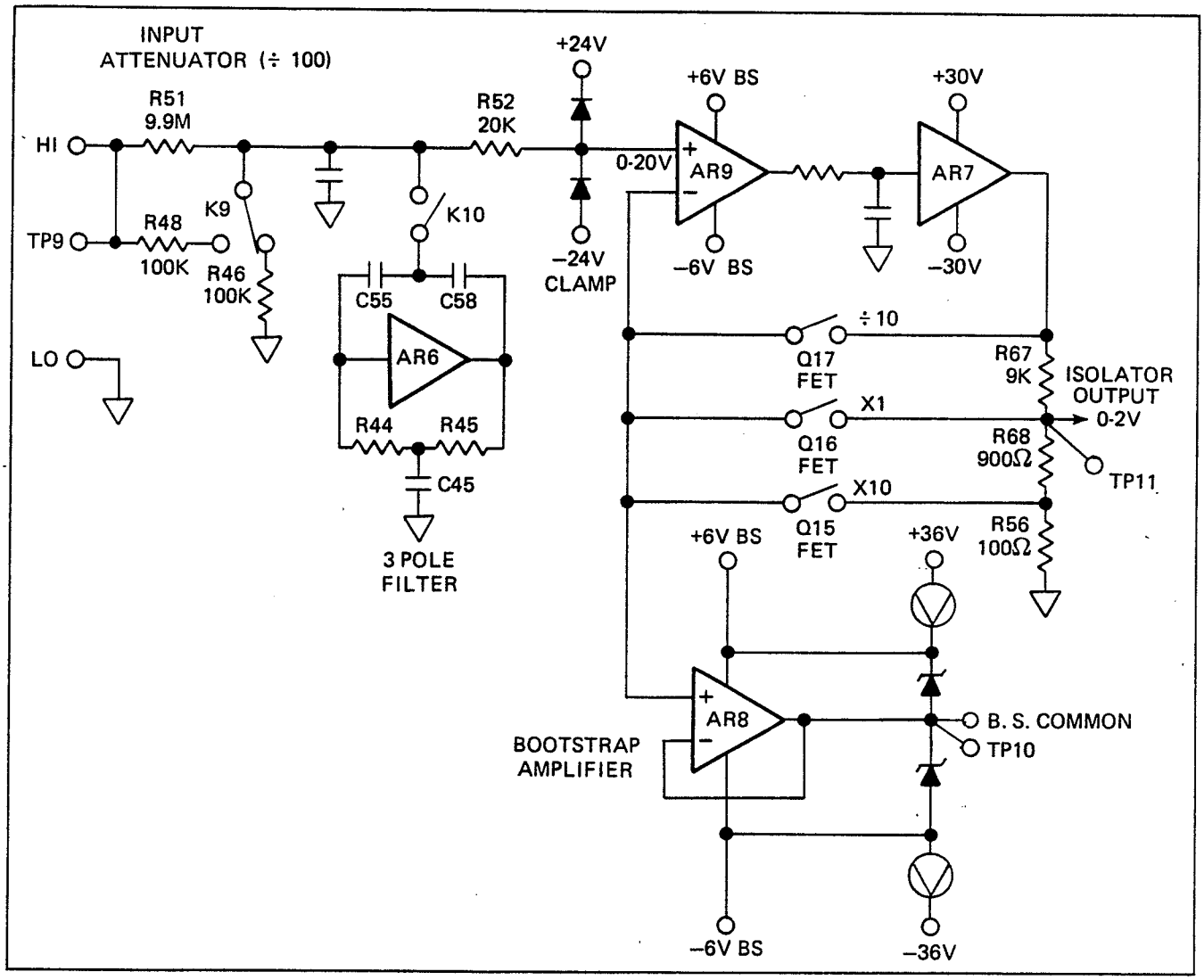


Figure 4.3 - Isolator and Bootstrap Amplifier

one volt full scale; filtering the signal to reduce unwanted noise; isolating the source from loading effects. The DC signal conditioning is performed by the Input Attenuator, Isolator, and Filter. A simplified diagram of this circuit is shown in Figure 4.3. The complete block diagram showing the relationship to other parts of the analog section is shown in Figure 4.2.

4.3.3.2 The DC signal applied to the DMM INPUT terminals is routed through the reference relay K13 and AC relay K12 to the DC input attenuator. If the .1,1 and 10 volt range is selected, the Attenuator relay K9 is energized and the input voltage is routed with no attenuation to the Isolator input. In this mode R48 parallels R51. This provides overload current limiting and forms part of the three-pole active filter. If the 100 or 1K volt ranges are selected, K9 is de-energized, completing a voltage divider of R51 and R46, attenuating the input signal 100:1 before application to the Isolator.

4.3.3.3 A User selectable three-pole active filter is switched in or out of the circuit at the Isolator input by relay K10. The filter consists of op-amp AR6, capacitors C45, C55, C58 and resistors R44, R45. Relay K10 can be enabled either via the keyboard or GPIB. The filter provides attenuation of noise frequencies above 10 Hz. Filter response is at least 35 dB down at 50 Hz and attenuates 18 dB/Octave to –60 dB or greater.

4.3.4 Isolator.

4.3.4.1 The Isolator contains an Input-Clamp, a high open-loop gain amplifier, bootstrap amplifier, and a gain switching network controlled by the range and function logic. A simplified diagram is presented in Figure 4.3 and the Isolator Range chart is shown in Table 4.3.

Table 4.3 - Isolator Range Chart

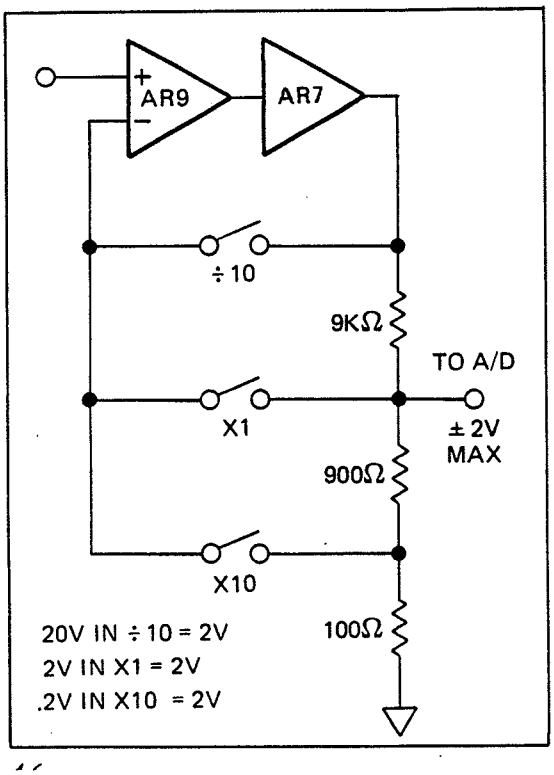
RANGE	K9	Q16	Q15	Q17	ISOLATOR GAIN
	÷ 100	X1	X10	÷ 10	
.1V	■		■		10
1V	■	■			1
10V	■			■	.1
100V		■			1
1000V				■	.1

■ RELAY ENERGIZED OR FET SWITCH ON.

4.3.4.2 The Isolator accepts varying voltages at its input from zero to ± 20 VDC, depending on the signal input and the range selected. The amplifier is non-inverting with a closed loop gain of 10, 1 or 0.1 depending on the DMM range selected. Inputs are thus scaled to ± 1 volt full scale level (± 2 volts with 100% over-range) and applied to the Digitizer. Input overloads are clamped at ± 24 volts.

4.3.4.3 The non-inverting configuration combined with the bootstrap amplifier increases the input resistance of the Isolator to over 1000 megohms. A high open loop gain is achieved by the use of two operational amplifiers, AR9 and AR7. The output of AR7 is applied to a feedback network consisting of R67, R68 and R56. Listed next is Table 4.4, which charts scale factors for the Isolator gain-switching (or attenuation) and Figure 4.3 shows a simplified diagram of the Isolator feedback network.

Table 4.4 - Isolator Gain Switching



When FET switch Q17 is closed, the output of AR7 is connected directly to the inverting input of AR9 as negative feedback. The closed loop gain to the output of AR7 is ONE, but since the output is tapped from the junction of R67 and R68, the overall Isolator gain is 0.1. When Q17 is closed, the overall gain is ONE and closing Q15 provides a gain of 10.

4.3.4.4 The BOOTSTRAP amplifier, AR8 and associated components, senses the Isolator feedback voltage (which tracks the input) and provides bootstrapped voltages (BSV) approximately 6 volts higher and 6 volts lower than the input to power AR9. The ± BSV on AR9 tracks the input to the Isolator which increases its input resistance above the level achievable without BSV. The output from AR7 (BS COMMON) drives the input bias current network to prevent it from shunting the input resistance.

4.3.5 Ohms Function.

4.3.5.1 The resistance measurement system shown in Figures 4.4 and 4.5 contain the ohms amplifier, voltage reference, current source, open input clamp and input over-voltage clamp. In operation, a fixed and stable current source is generated for each range and the current is fed through the resistance to be measured. The voltage drop across the resistor is proportional to the unknown resistance Rx. This voltage is read by the DMM and displayed as kilohms on the display. The current supplied provides a full scale DMM reading when the unknown resistance is equal to the range selected. For an example, the measuring of 10 kilohms on the 10 K range produces a DMM readout of 10.0000.

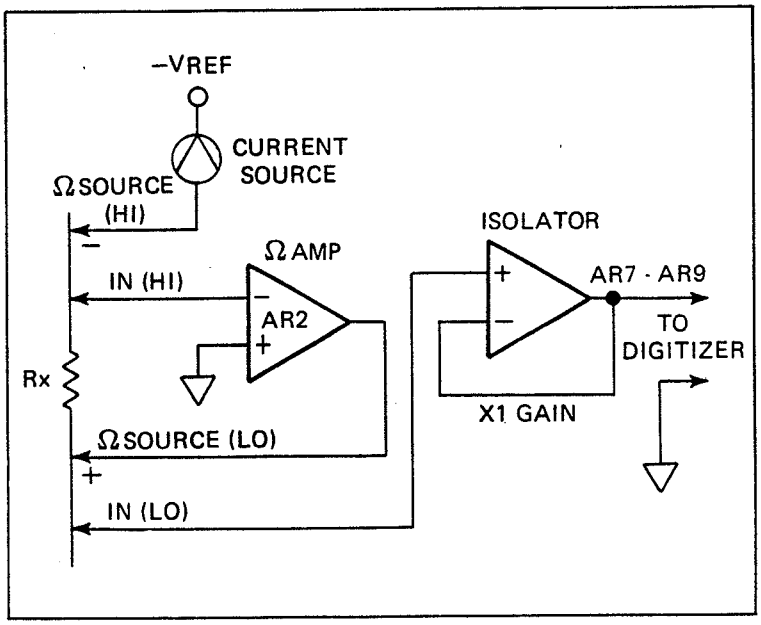


Figure 4.4 - Resistance Measurement System

4.3.5.2 The Ohms current source utilizes an accurate reference voltage to generate a reference current source through the resistor divider and current switching network, refer to Figure 4.5. An open input-clamp is also part of the ohms converter circuit. The ohms voltage reference is a 7 volt temperature-stabilized zener, VR2. The 7 volt reference is buffered by the ohms current source generator op-amp AR1. The current through darlington transistor pair Q7 and Q8 is determined by R31 and R35. This network supplies 1 mA or 10 mA to the current-divider network. Relay K7 switches R35 in parallel with R31 to generate the 10 mA current source. The lower Ω source currents required for the 10K, 100K, 1000K and 10,000KΩ ranges are established by dividing the Ohms CURRENT SOURCE output. The current divider consists of R25, R27, R28, R29 and R33 and the division is controlled by range relays K2-K6. The ohms ranges, current sources and the range relays are shown in Table 4.4.

4.3.5.3 \The Open-Input clamp protects the user's external input from voltage increases when the ohms terminals are not provided with a resistive load, or during range overload. The input open circuit voltage is clamped at −6 volts maximum by Q3, Q5 and transistor array U3. U3 clamps the base of Q7 to −30 volts thereby turning off the current source through Q8 during overload. CR2, Q8 and VR3 protect the current source from voltages applied at the input terminals.

Table 4.5 - Ohms Range, Relay and I Source

RANGE	K2	K3	K4	K5	K6	K7	Ω SOURCE CURRENT
.1K					■	■	10 ma
1K					■		1 ma
10K	■		■				100 μa
100K		■	■				10 μa
1000K			■				1 μa
10000K				■			100 na

■ ENERGIZED

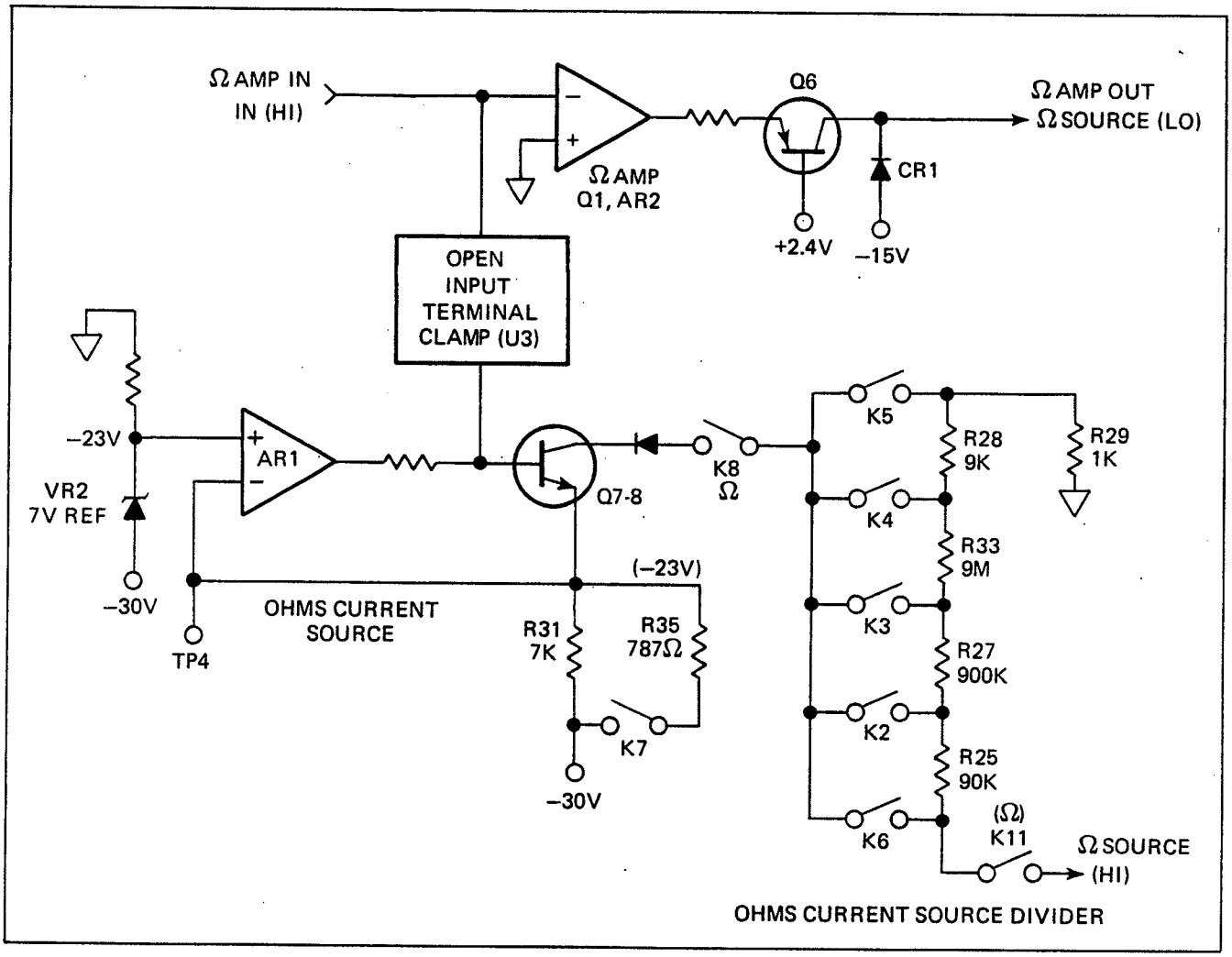


Figure 4.5 - Simplified Ohms Converter

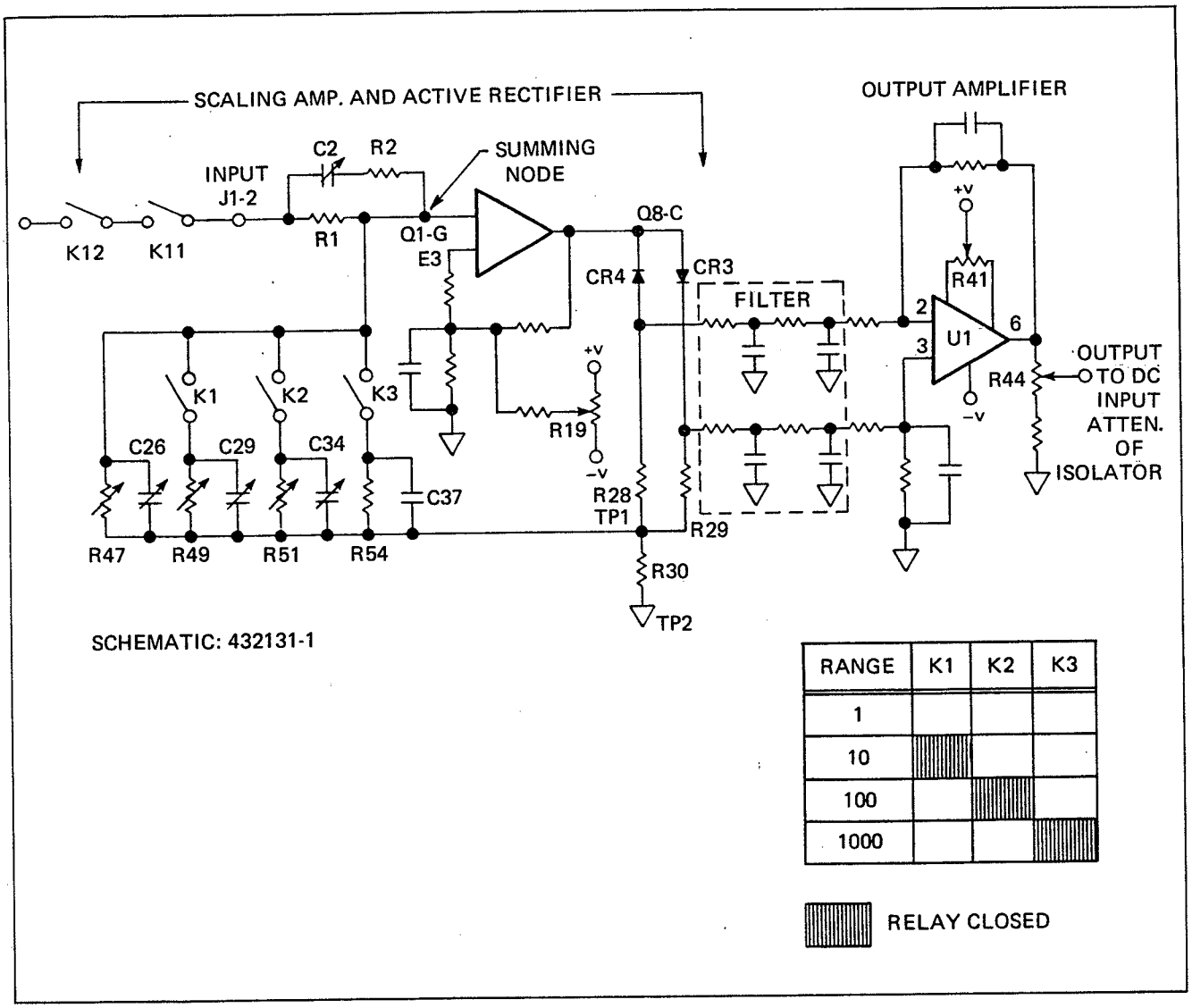


Figure 4.6 - Averaging AC Converter

4.3.6 Averaging AC Converter (Model 5005)

4.3.6.1 The Model 5005 DMM features an averaging AC to DC converter that is assembled in a separate PCB located in section 2A of the DMM Sectional drawing Fig. 4.1, and plugs into connectors J1 and J2 on the motherboard. The AC converter is configured with a Scaling Amplifier Q1-Q8; Active Rectifier section CR3 and CR4; and a ripple filter network. The converter output amplifier employs U1 op-amp to generate –1VDC full scale.

4.3.6.2 From the inputs terminals, the AC input signal is switched to C1 coupling capacitor, through the AC relay K12 (energized) and through the ohms relay K11 (de-energized). The AC signal continues through the RC network of R1-R2-C2 to the input the summing node of the Scaling Amplifier. A simplified drawing of the AC assembly is shown in Fig. 4.6, a take-off from schematic drawing 432131-1.

4.3.6.3 The Scaling amplifier Input resistor R1, and sellectable feedback resistors control gain of each range. Range relays K1-K3 select the feedback resistors for each range. The Scaling amplifier attenuates the input signal in the 1, 10, 100 and 1 KV ranges. Feedback on the 1V range is through the permanently connected resistor R46/47. The 10, 100, and 1 KV ranges have relay selected feedback that parallel the 2V network through R48&49, R50/51/52, and R53/54/55 respectfully. The output from the scaling amplifier is 1V for full scale in each range. The relay chart shown in Fig. 4.6, presents the relay states for each range selected.

4.3.6.4 The Scaling amplifier input is protected from overload voltages by diode clamp CR1 and CR2.

4.3.6.5 The active rectifier configuration has two distinct polarity feedback paths; the feedback path consisting of CR3 and R29 conducts current when the output of the amplifier is positive and the CR4 - R28 path conducts when the amplifier output is negative. The two currents are combined across resistor R30 and the resulting AC signal is fed through the range feedback network to the input summing node of the scaling amplifier. Two half-wave signals of opposite polarities are developed across resistors R28 and R29 for each full-wave input. These signals are filtered to a DC level and amplified by a gain of ten by the differential output amplifier U1 and routed to the DC input attenuator of the isolator. (−1V for full scale).

4.3.7 RMS AC Converter (Model 5006)

4.3.7.1 The Model 5006 DMM features an RMS AC to DC converter that is assembled on a separate PCB and located in section 1A of the DMM Section drawing Figure 4.1. The PCB plugs into connectors J1 and J2 on the motherboard. The RMS converter is configured with a Scaling Amplifier – Q3, AR1, range switching and input clamp networks; active DC Rectifier–Amplifier Q4 through Q9, CR1 and CR2; Logarthmic (log) Amplifier - Q10 through Q14; RMS Output Amplifier Circuitry - AR2, DC attenuator, and a ripple filter.

4.3.7.2 From the DMM input terminals, the AC signal is routed to C25 coupling capacitor, through the AC relay K12 (energized) and through the Ohms relay K11 (De-energized). The AC signal continues through the RC network of R57 and associated components to the input of the scaling amplifier. A simplified drawing of the RMS assembly is shown in Figure 4.7, a take-off from schematic drawing 432131.

4.3.7.3 The Scaling Amplifier (differential dual FET input, transistor Q3 and op-amp AR1) is an inverting operational amplifier that conditions the input signal and generates a full scale output of 1 volt AC in the 1V range. Signal attenuation for the 10, 100 and 1 KV ranges are developed by feedback resistors R7/8, R5/6 and R2/3 through range relays K3, K2 and K1 in the feedback circuit of AR1. The AC output signal from AR1 Pin 6 is routed via R19-5K and R24-20K resistor to the summing node of the log amplifier Q11 and to the input of Q5 the RMS converter circuitry. The Scaling Amplifier inputs (at Q3) is protected from overload voltages by transistors Q1, Q2, A15, and Q16 wired as diodes and connected as positive and negative voltage limiting clamps.

4.3.7.4 The Active Rectifier circuitry, which includes Q4 through Q9, CR1 and CR2, is configured as an op-amp with dual polarity feedback routes. One feedback route through CR1 and R21 conducts during the negative voltage excursions from the amplifier. During the positive voltage excursions, CR2 via R23 completes the feedback path to differential amplifier Q5. This half-wave positive-rectified signal also travels via R32-10K to the summing node of the log amplifier Q11; the input to the RMS converter circuitry.

4.3.7.5 The RMS converter (log amplifier Q11, Q12 and Q13; log feedback loop Q10A and Q14B) is configured as an operational amplifier with a logarithmic feedback loop. The output from the log amplifier (Q13 collector) is the log of the total summing node input to Q11 received via the Active rectifier, Scaling amplifier and the log exponential feedback voltage developed across Q14A and Q10A, and is proportional to the log of the rectified signal current.

4.3.7.6 The output from the log amplifier also drives the input network to AR2 op-amp that is identical to the log amplifier feedback loop which consists of Q14B and Q10B. This input network supplies current to the summing node of the output amplifier AR2 and converts the log amplifier output Q13 to an RMS current, with the AC component bypassed through C20. The DC component is fed through Q10B to the input of the output amplifier AR2. This current is converted to a 5 volt RMS voltage (for a full-scale input) at the output of the driver amplifier AR2. The RMS construction through the log amplifier can be itemized as noted next:

a) Q14B squares the signal - C20 averages it.
b) AR2 performs the averaging of the squared signal.
c) Q10B extracts the square root.

From the output driver amplifier, the 5 VRMS is filtered and attenuated in the output RC network to deliver a 1 volt full-scale level signal that is routed to the DC signal conditioner input.

4.3.7.7 Measurements may be made in the AC coupled mode (standard) or DC coupled mode (AC + DC). In the DC coupled mode S2 is switched, applying a short across C25 and S1 is switched, applying a short across C15. DC blocking capacitors C25 and C15 are active in the AC coupled mode only.

4.4 QUANTIZED FEEDBACK A/D CONVERTER.

4.4.1 General.

4.4.1.1 The A/D Converter uses a quantized feedback (QF) conversion technique to convert the analog output from the Isolator to a BCD format for further processing and display.

4.4.1.2 The A/D Converter hardware is located in Section 5 of the PCB assembly. The converter consists of A/D Analog Processor (U11), Digital Counter and Control I.C. (U10), Measure/Zero (M/Z) switch U26, Input Buffer AR5, Auto-Zero Buffer AR3, Auto-Zero switch Q9, Digit Mode switch

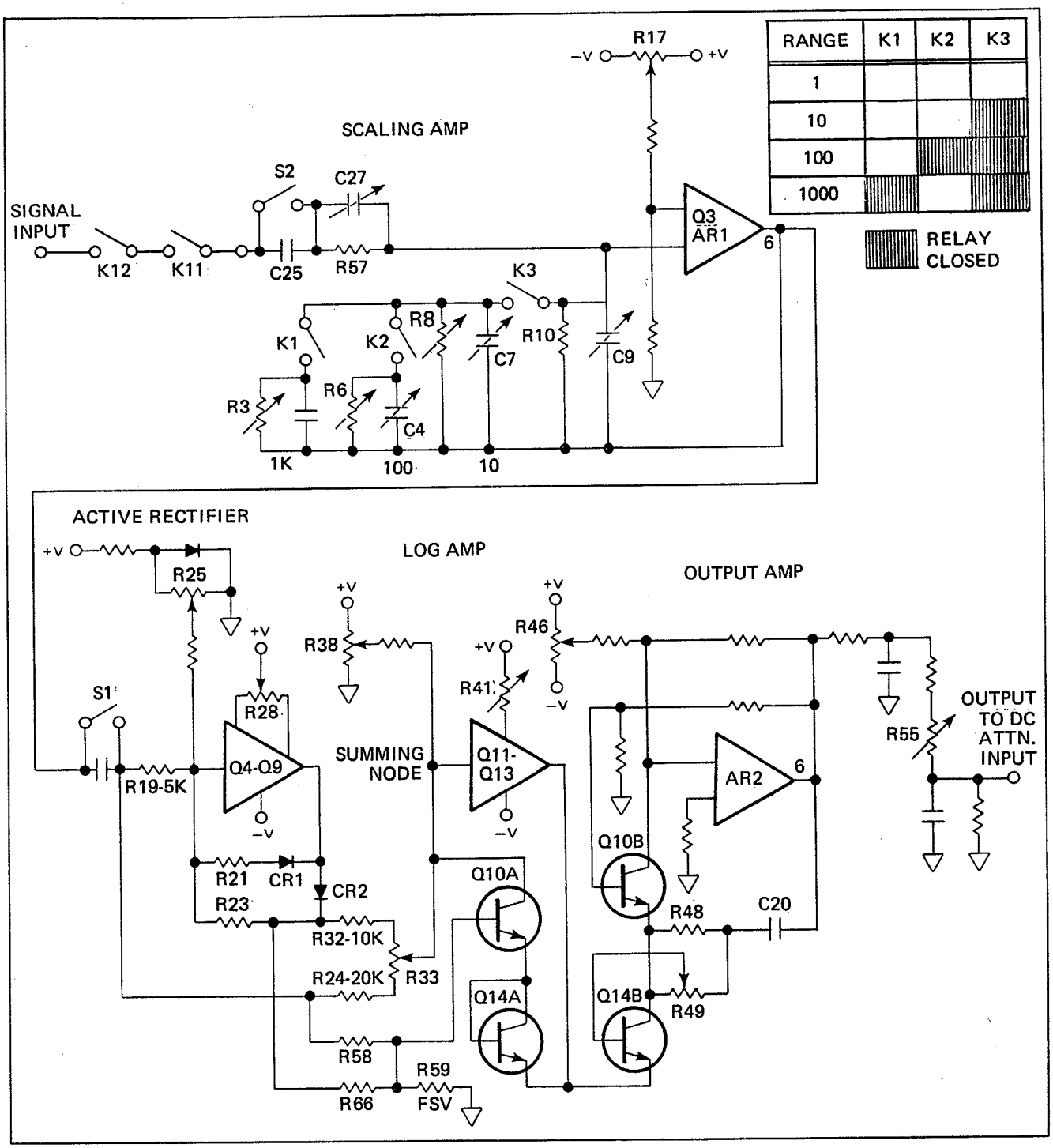


Figure 4.7 - RMS AC Converter

Q10, Voltage Reference VR1, and Opto-isolator drivers U9/U17. A simplified diagram of the Analog Processor and supporting external circuitry is shown in Figure 4.8 where designators and circled numbers relate to the A/D schematic at page 6-9. A block diagram of the A/D Digital Counter and Control is presented in Figure 4.9.

4.4.1.3 The A/D conversion is performed by two LSI circuits - a charge-balancing Analog Processor (U11) and a proprietary Digital counter and control IC (U10), that contains all the digital circuitry for the 'quantized feedback' system. The Analog Processor contains a bipolar comparator, bipolar integrating amplifier, buffer amplifiers and analog

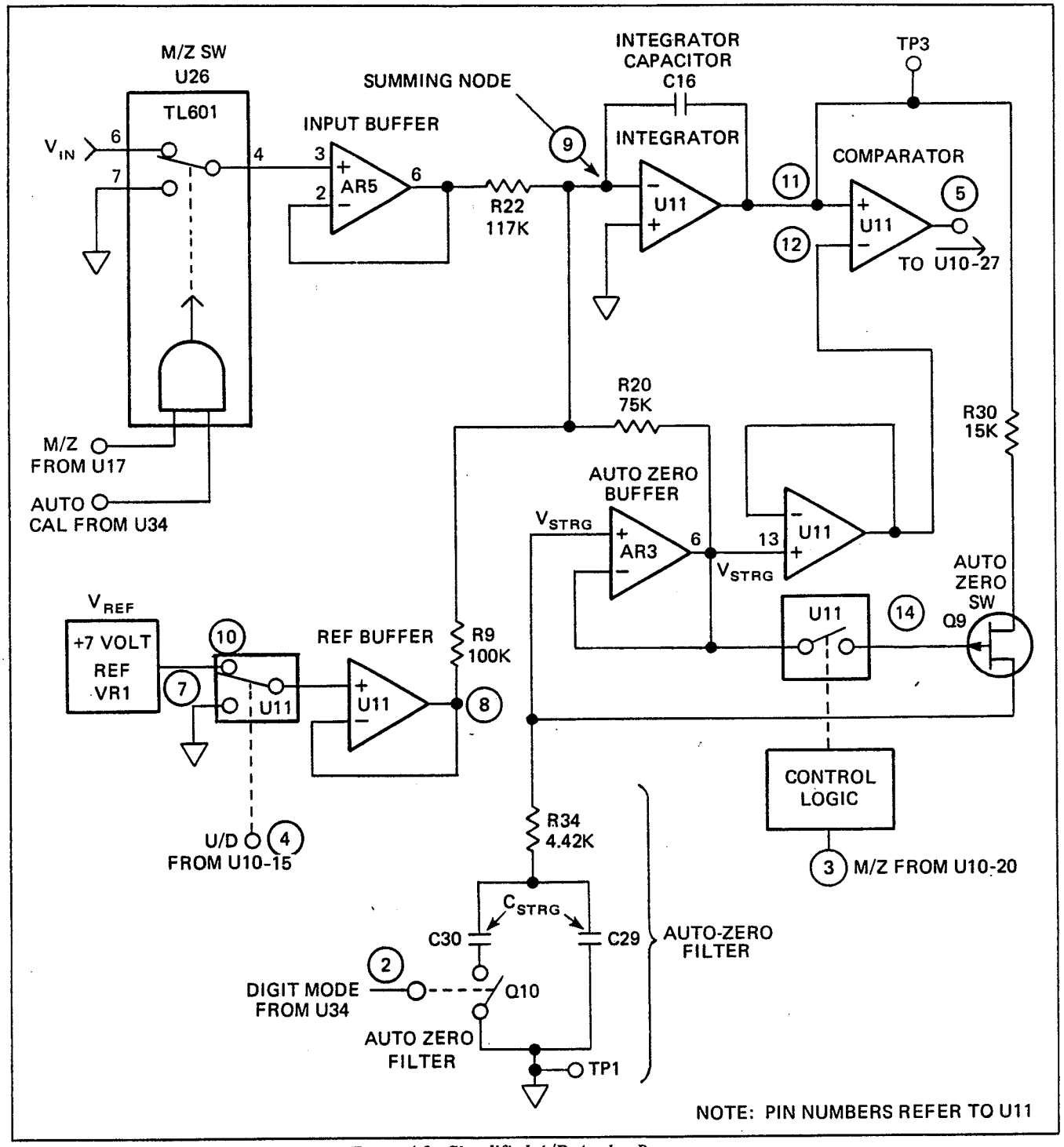


Figure 4.8 - Simplified A/D Analog Processor

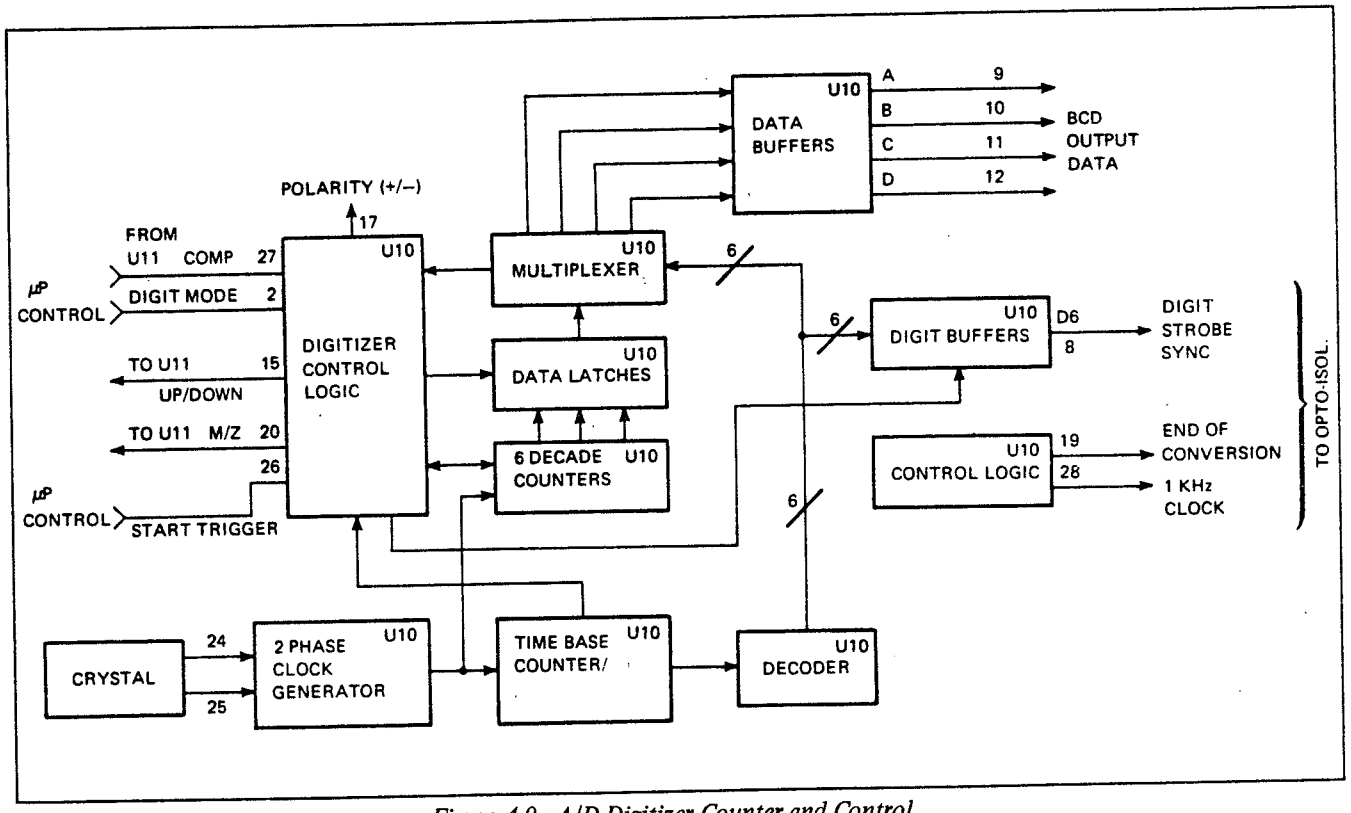


Figure 4.9 - A/D Digitizer Counter and Control

switches. External Buffer amplifiers AR5 and AR3, measure/zero (M/Z) switch U26 and auto-zero switch (Q9) are used to improve performance of the Analog Processor. The Digital Control I.C. is a synchronous digital processor and combines the time-base generation, counting, data multiplexing and random logic necessary to control the Analog Processor. A stable 7 volt reference voltage for the A/D converter is supplied by VR1.

4.4.2 Time Base Generation.

4.4.2.1 MEASURE/ZERO (M/Z) SIGNAL.

4.4.2.1.1 Basic timing signals for the A/D Converter are generated by the 2-Phase Clock Generator and Time-base Counter in U10. The Clock Generator, controlled by an external crystal, supplies a two-phase output at a 2.4576 MHz frequency (2.048 MHz in 50 Hz instruments) to the Time-base counter. In 60 Hz instruments operating in the 5-1/2 digit mode, the Time-base counter divides the clock frequency into sampling periods of 614,400 pulses (250 milliseconds). A period of 409,600 pulses (166.67 ms) is defined as the Measure Interval and 204,800 pulses (83.33 ms) as the Auto-zero interval. When operating in the 4-1/2 digit mode the Measure Interval is 16.67 ms and the Auto-zero period is 8.33 ms. The resulting measure/zero (M/Z) waveform, shown in Figure 4.10, is applied to the analog processor. When the logic level on the START TRIGGER line is held low, the M/Z waveform is generated continuously and the DMM is taking measurements continuously at a rate of 4 readings/sec (60 Hz instrument, 5-1/2 Digit mode) or 40 readings/sec (60 Hz instrument, 4-1/2 Digit mode). When operating the DMM in the Hold/Command (triggered reading) mode, a logic high on the START TRIGGER line holds the system in the Auto-zero mode. A negative going pulse on this line initiates one measurement cycle.

4.4.2.2 UP/DN CONTROL SIGNAL.

4.4.2.2.1 The up/down (U/D) control signal to the Analog Processor is also derived from the Time-base counter. This control signal has a period of 160 clock pulses. During the Auto-zero mode the U/D waveform has a 50% duty cycle (logic high for 80 counts and logic low for 80 counts). During the Measure interval the Digitizer Control logic examines the output of the comparator in the Analog Processor once each 160 clock pulses. If the comparator output is high, the UP/DN control will be high for 10 clock pulses and low for 150 clock pulses during the next 160 clock pulses. If the comparator output is low, the U/D control will be high for 150 pulses and low for 10 pulses. How the U/D control is used to control the Analog Processor is discussed in the following paragraphs.

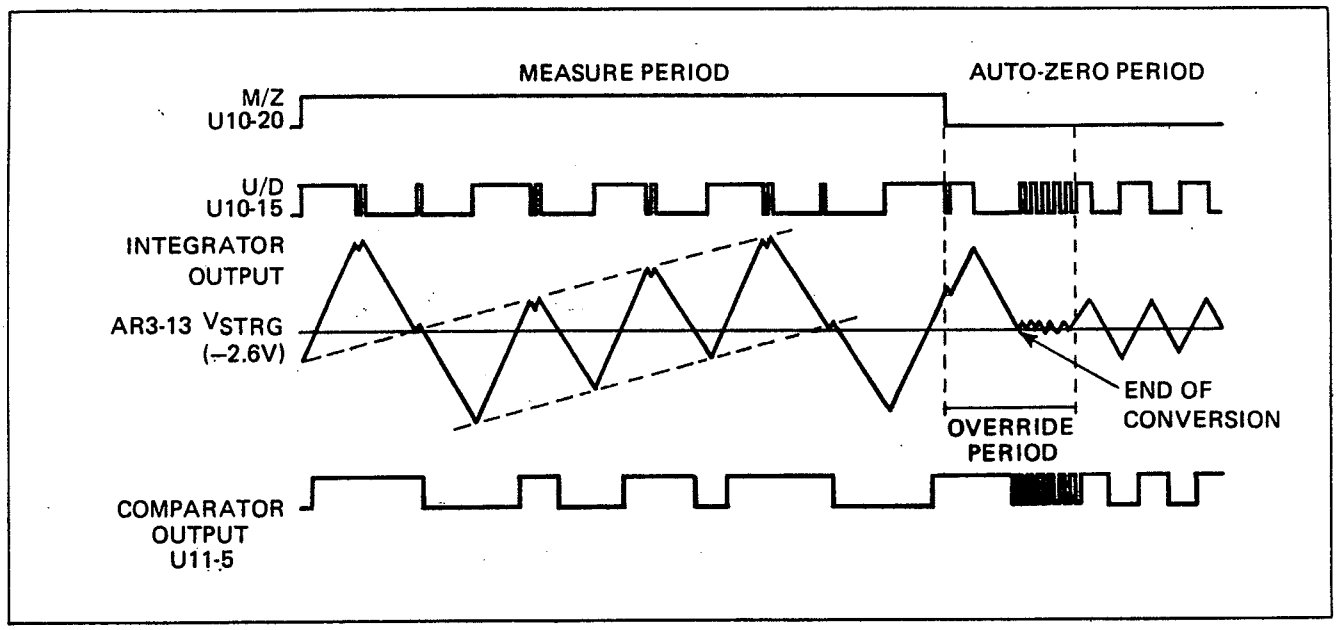


Figure 4.10 - Typical A/D Converter Waveforms

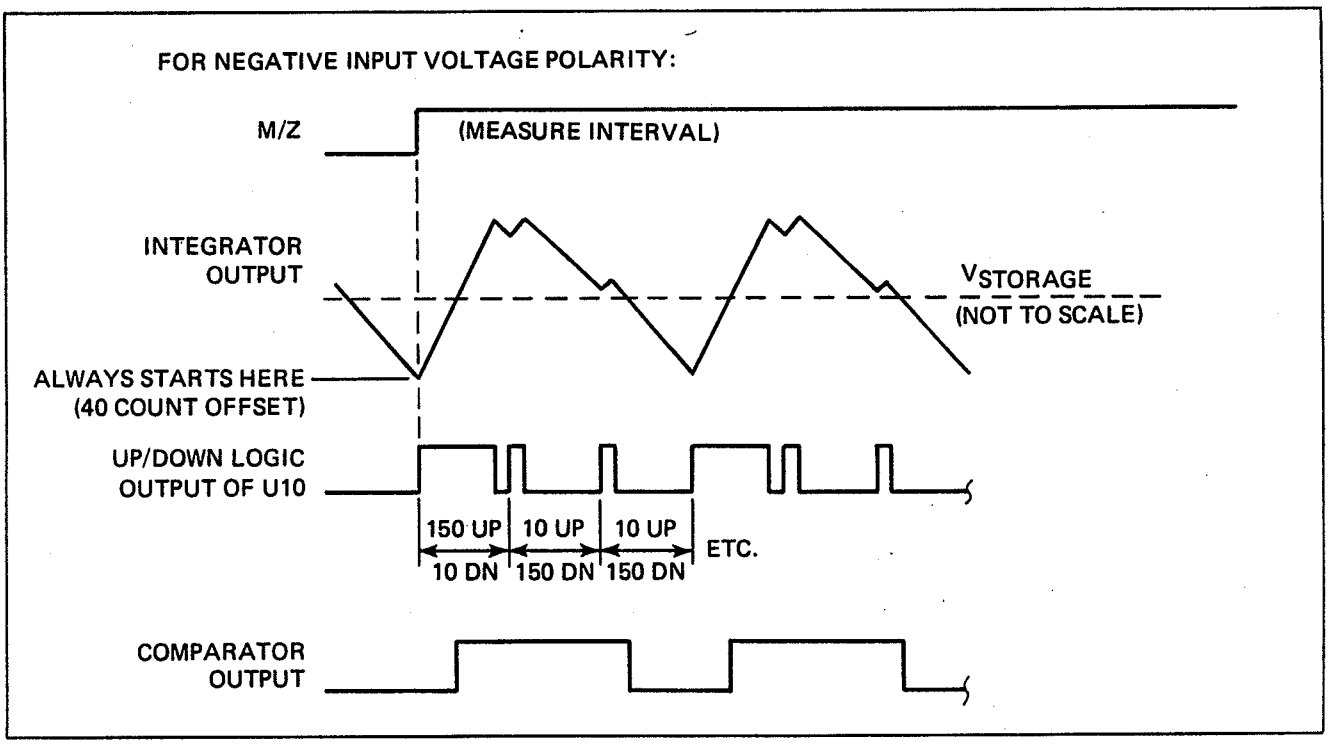


Figure 4.11 - Waveforms at Beginning of Measure Interval for Negative Input

4.4.3 Auto-Zero Interval.

4.4.3.1 Referring to Figure 4.8, during the Auto-zero (A/Z) interval the input of AR5 (Input Buffer) is switched from the Isolator output to analog common by M/Z switch U26. Auto-zero switch Q9 is enabled and connects the Integrator output to Auto-zero filter capacitors C29 and C30, and the input of Auto-zero buffer AR3. Both switches are controlled by the M/Z signal from the Digital Control IC, U10. The U/D control signal, with its 50% duty cycle, alternately switches the input of the Reference Buffer between Analog Common and the 7 volt reference, VR1. When the U/D control is low, the Reference Buffer output is equal to +7 volts; when the U/D control is high, the Reference Buffer output is zero. The Integrator input current (pin 9 of U11) is a summation of currents from the Input Buffer, Reference Buffer and Auto-Zero Buffer through resistors R22, R9 and R20 respectively. The average current through R9 is equal to one-half the Reference Voltage divided by the value of R9, $\frac{(VREF)}{2R9}$, because the reference current is flowing through R9 half of the time. The Auto-zero Buffer supplies a current through R20 equal to the voltage on the Auto-zero Filter capacitors divided by R20. The output of the Integrator is applied to the Auto Zero Filter capacitors C29 and C30 through R30, Q9 and R34, and the capacitors charge to a voltage proportional to the average value of the input currents (approx. −2.6V). This voltage is negative because of the inverting action of the Integrator. C29 stores the Integrator output in the 4-1/2 Digit mode, and C30 is switched in parallel by Q10 when the 5-1/2 Digit mode is selected to provide a longer time constant. Note that the voltage, Vstrg, at the output of AR3 is also applied to one input of the comparator through an internal Buffer Amplifier. This voltage remains on the comparator during the Measure Interval and establishes the comparator threshold at Vstrg (−2.6V).

4.4.3.2 The loop around the Integrator reaches equilibrium when the sum of the currents into the Integrator summing node equal zero. The voltage on the Filter capacitors (Cstrg) remains at approximately −2.6V when the Auto-zero switch Q9 opens at the end of the AZ interval because of the high input impedance of AR3. The BCD counters in U10 are also reset to zero by the last clock pulse of the Auto-Zero interval.

4.4.4 Measure Interval.

4.4.4.1 At the start of the Measure Interval; (a) the M/Z control goes high, switching the Isolator output to the Input Buffer AR5 through M/Z switch U26, (b) Auto-Zero switch Q9 is switched OFF, disconnecting the Integrator output from the Auto-Zero Filter capacitors, (c) U/D control is high, switching the Reference Buffer input to Analog Common, and (d) the Integrator output is slightly more negative than Vstrg (see Figure 4.11). At this time, the only inputs to the Integrator are Vstrg and the input signal from the Isolator (buffered by AR5). With only these two inputs, the Integrator output will always move in a positive going direction, independent of the polarity of the signal from the Isolator. As the Integrator output moves away from Vstrg, the comparator senses the output of the Integrator and compares it to Vstrg on the other Comparator input (pin 12 of U10). The comparator output transmits the sense of deviation of the Integrator output from Vstrg to the Control Logic circuits in U10. The Control Logic circuit generates the UP/DN control signal as described in paragraph 4.4.2.2 and shown in Figure 4.10 and 4.11. The effect of the two duty cycles (10 up, 150 down or 150 up, 10 down) is to source or sink a net 140 clock pulses of charge to integrator capacitor C16, thus driving the Integrator output toward Vstrg and accumulate a net 140 counts in the up/down counters. The charge is supplied by the current through R9 from the buffered Reference voltage. Charge is added to C16 when the Reference Voltage is applied to R20 and subtracted when the Reference voltage at the output of the Reference Buffer is zero. The net amount of charge required to keep the Integrator output at Vstrg during the Measure Interval is measured by the Up/Down Counter in the Digital I.C. The BCD count at the end of conversion equals the number of charge parcels necessary to cancel the input voltage and the resulting digital count is proportional to the analog voltage.

4.4.5 Over-Ride Interval.

4.4.5.1 At the end of the Measure Interval the total counts accumulated by the counter will be a multiple of 140. A residual voltage on Integrator capacitor C16 represents the remaining unresolved portion of the input. This voltage is cancelled and the corresponding counts accumulated during